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IN THE U.S. PATENT AND TRADEMARK OFFICE

Appl. No.:	10/691,252
Applicant:	Michael Buchmann
Filed:	October 22, 2003
TC/AU:	2838
Examiner:	Bao Q. Vu
Docket No.:	890A.0001.U1(US)
Customer No.	29683

Title: Voltage Multiplier with Charge Recovery

Mail Stop Appeal Brief - Patents
Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

APPELLANT'S APPEAL BRIEF

Sir:

Commensurate with the Notice of Appeal filed on July 16, 2007, Applicant/Appellant hereby submits this Appeal Brief to the Board of Patent Appeals and Interferences (hereinafter, the Board) under 37 C.F.R. §41.31. The Patent Office reopened prosecution on July 16, 2007, in response to the Appeal Brief filed on 27 November 2006. That Appeal Brief had been filed on November 20, 2006, with the Notice of Appeal filed on 5 September 2006, in a submission to the Board of Patent Appeals and Interferences (hereinafter, the Board) under 37 C.F.R. §41.31. In response to an earlier Appeal Brief filed on December 27, 2005, the Patent Office reopened prosecution with a non-final office action dated March 1, 2006. Applicant believes that no new Appeal Brief Fee is due. Please charge Deposit Account No. 50-1924 as appropriate.

This Appeal Brief is filed between the second and third months after the filing of the Notice of Appeal. As such, the undersigned representative believes that a one-month

extension of time fee is due and, thusly, petitions for a one month extension of time under 37 C.F.R. §1.136(a) or (b) that may be required to avoid dismissal of this appeal. Please charge Deposit Account No. 50-1924 as appropriate.

(1) REAL PARTY IN INTEREST

The real party in interest (RPI) is Nokia Corporation of Espoo, Finland, as indicated in an assignment of the U.S. application recorded on October 22, 2003 at reel 014638 and frame 0238.

(2) RELATED APPEALS AND INTERFERENCES

There are no other pending appeals or interferences of which the undersigned representative and assignee/RPI is aware that will directly affect, be directly affected by or have a bearing on the Board's decision in this appeal.

(3) STATUS OF CLAIMS

Claims 1-8 are pending in this appeal and stand finally rejected. Claims 1-8 are reproduced in an Appendix accompanying this Brief as those claims stood finally rejected by the Office Action dated 16 July 2007.

(4) STATUS OF AMENDMENTS

No amendments are pending. All amendments have been previously entered.

(5) SUMMARY OF CLAIMED SUBJECT MATTER

Reference may be had to FIGS. 1, 10a, 10b, and 11 for this Summary. Independent claim 1 is directed to a capacitive voltage multiplier (FIG. 1, FIG. 11) for generating voltage pulses that are higher than the supply voltage (e.g., the voltage on input 31; see page 7, lines 20-23). The multiplier (FIG. 1, FIG. 11) includes a switching capacitor circuit (21) coupled between input (31) and output (32) terminals of the multiplier. The switching capacitor circuit (21) is provided with capacitors (e.g., capacitors 11, 12, 13 of FIG. 11) and is further provided with switches (e.g., switches 1-8 of FIG. 11) for charging the capacitors (e.g., capacitors 11, 12, 13 in FIG. 11) in parallel and discharging them in series in order to deliver a high voltage pulse. See also FIGS. 10a and 10b regarding operating switches S1-S12 in order to charge capacitors C1 through C4 in parallel and discharge the capacitors C1 through C4 in series. The multiplier (FIG. 1, FIG. 11) further includes a diode chain circuit (22) coupled between the input (31) and output (32) terminals of the multiplier (FIG. 1, FIG. 11), said diode chain circuit (22) includes a diode-chain (e.g., diodes 41, 42, 43 and 102 of FIG. 11). The diode chain circuit (22) includes pumping capacitors (e.g., capacitors 51, 52, and 53 of FIG. 11) for delivering high voltage current. See also the description from page 6, line 6 to page 8, line 3.

(6) GROUNDS OF REJECTION TO BE REVIEWED ON APPEAL

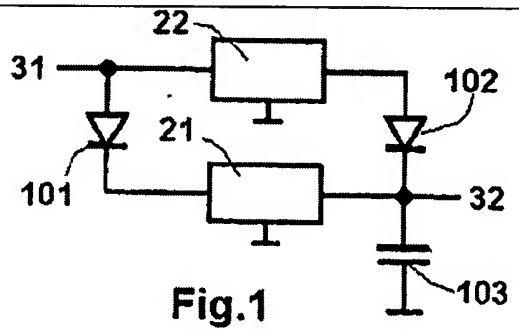
The only ground for rejection presented for review by the Board is whether claims 1-8 are unpatentable as being obvious under 35 U.S.C. §103(a) by Kowshik, U.S. Patent No. 5,625,544, in view of Soneda, U.S. Patent No. 5,856,918.

(7) ARGUMENT

Claims 1-8 stand rejected as being obvious under 35 U.S.C. §103(a) by Kowshik, U.S. Patent No. 5,625,544, in view of Soneda, U.S. Patent No. 5,856,918. This is the sole ground for rejection. Claim 1 is the sole independent claim.

CLAIM 1

A portion of independent claim 1 is shown on the left side of the following table. On the right side, a portion of FIG. 1 of the present application is shown for ease of reference. FIG. 11 shows examples of elements 21 and 22 in greater detail.

Capacitive voltage multiplier ..., wherein the multiplier comprises a switching capacitor circuit (21) coupled between input (31) and output (32) terminals of the multiplier, said switching capacitor circuit (21) provided with capacitors and switches for charging the capacitors in parallel and discharging them in series in order to deliver a high voltage pulse, characterised in that the multiplier further comprises a diode chain circuit (22) coupled between said input (31) and output (32) terminals of the multiplier, said diode chain circuit (22) comprising a diode-chain and pumping capacitors for delivering high voltage current.	 Fig.1

Applicant reads Kowshik as providing charge pump circuits having an output stage in series with "N stages of diode-capacitor voltage multipliers clocked so as to convert a low voltage received from a supply voltage to a high voltage at an output terminal thereof employs an output stage to improve the efficiency of the charge pump. The output stage includes first and second legs each coupled to the output terminal, where the first leg provides current to the output terminal during low transitions of the clock signal and the second stage provides current to the output terminal during high transitions of the clock signal," Kowshik, column 1, lines 50-60. That the output stage is serially coupled to the stages of diode-capacitor voltage multipliers can be seen in Figs. 2 and 2A of Kowshik.

Kowshik does not allow charge pump circuits to be implemented in parallel, see Figs. 3 and 3A of Kowshik and Kowshik, column 3, lines 35-53. Specifically, Kowshik states that "[w]here it is desired to generate even greater currents to output terminal V_{pp}, a plurality of circuits 200 may be connected in parallel, where each of circuits 200 receives its own clock signal and an associated high-transition non-overlapping clock signal," Kowshik, column 3, lines 35-39. Further, Kowshik shows, in Figure 3, "two charge pump circuits 200a and 200b, where circuits 200a and 200b are each substantially identical in structure and operation to circuit 200" (column 3, lines 40-43).

However, none of the circuits shown and described in Kowshik discloses or implies a capacitive voltage multiplier comprising a switching capacitor circuit (21) and a diode chain circuit (22), each of which is coupled between input (31) and output (32) terminals of the multiplier, as recited in independent claim 1.

Soneda, U.S. Patent No. 5,856,918, describes a semiconductor-switch based circuit for charging capacitors in parallel and discharging them in series in the conventional well-known voltage multiplying manner, but using a novel capacitor control and clocking method.

Note that output ripple is reduced by continuously clocking the circuit and thereby continually charging capacitors in parallel and discharging them in series.

In the present invention ripple reduction is by a "continuously operated" (see the present claim 6) diode based voltage multiplier that is not charging capacitors in parallel and discharging them in series.

The operation of the Soneda circuit is thus different from the operation of the present invention.

What would the motivation be for one of ordinary skill in the art to modify Kowshik so as to incorporate the internal power supply circuit other than through impermissible hindsight reconstruction? Kowshik would add another circuit 200 to increase output current and makes no mention or suggestion of using any other circuit.

It is accordingly respectfully submitted that claim 1 and its dependent claims 2-8 are allowable over Kowshik in view of Soneda.

CLAIM 2

The Patent Office has not addressed the merits of claim 2. Claim 2 recites the following: "Capacitive voltage multiplier according to claim 1, characterised in that when high voltage pulse is desired in the switching capacitor circuit (21) the series coupling switches (odd) are activated by a control pulse and all other switches (even) are opened and that in stand-by mode (no pulse) the series coupling switches (odd) are open and all other switches (even) are closed in order to charge the pump capacitors from the supply voltage, and that charge sharing will occur with the charge including the load capacitance (103)."

Importantly, claim 2 recites the subject matter "that charge sharing will occur with the charge including the load capacitance (103)." See the following figure from Applicant's specification:

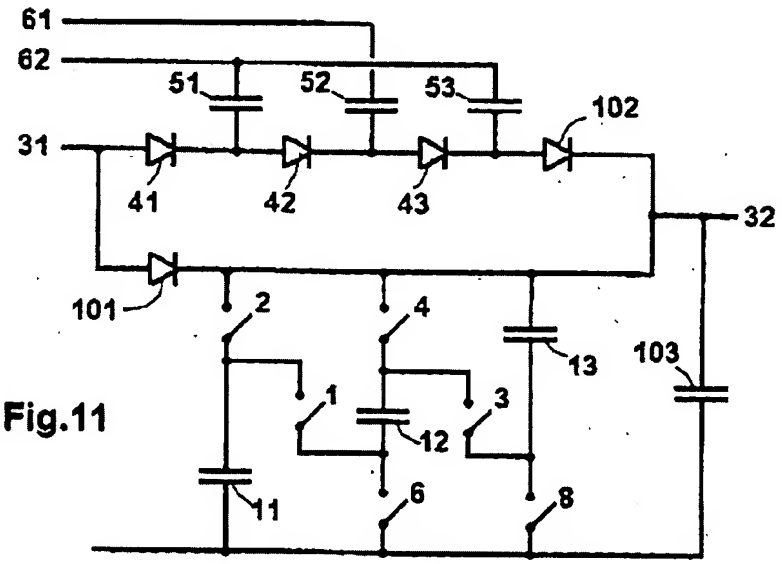


Fig.11

It can be seen that charge sharing between the load capacitance 103 and the capacitors 11-13 can occur, e.g., when the even switches are closed and the odd switches are open. In the present invention the voltage multiplier that charges capacitors in parallel and discharges them in series is not continuously clocked, only at the beginning of the output pulse, see the present claim 2 describing the single control pulse. Note also that nowhere in the Soneda specification is charge conservation an issue or even mentioned, whereas it is an advantageous feature in the present invention made possible by using only a single control pulse.

Kowshik does not disclose a switching capacitor circuit. As described above with regard to claim 2, charge sharing between the load capacitance 103 and the capacitors 11-13 can occur, e.g., when the even switches are closed and the odd switches are open.

CLAIM 3

The Patent Office has not addressed the merits of claim 3. Dependent claim 3 recites "Capacitive voltage multiplier according to claim 1, characterised in that the switches of the switching capacitor circuit (21) are MEMS switches."

The intended use of Soneda's "Internal Power Supply" using "Semiconductor switches" is to generate a needed higher programming voltage, typically 5 to 10 VDC, inside programmable memory circuits from the memory supply voltage, which typically is 5 VDC or less.

This higher programming voltage is an order of magnitude lower than the maximum output voltage of up to 100V (see our first claim) of the present invention that uses MEMS switches.

The possibility to use MEMS switches is never even mentioned by Soneda, perhaps because the conventional wisdom at the time of the invention, and still to a certain degree, is that MEMS switches cannot be used in continuous operation. To be able to use MEMS switches is novel.

Kowshik, U.S. Patent No. 5,625,544, describes a multi stage charge pump for voltage multiplying.

The Kowshik circuit includes a first and a second parallel leg that provides output current at opposite phases of the driving clock signal and if needed more legs can be used to increase the output current. In another embodiment two sub-legs are serially connected, and the output sub-leg provides output current at both phases of the driving clock signal.

The Kowshik circuitry indeed increases efficiency and gives a stable output like many other voltage multiplying circuits. But because all the embodiments Kowshik describes

employ diodes at the output, charge conservation cannot take place in the way as described in the present claim 6 of our invention.

The Kowshik invention is not in any embodiment similar to the present invention, nor can the present invention be considered obvious by studying the Kowshik circuitry. The Kowshik circuitry either uses serially connected legs or multiple symmetrical legs whereas the present invention never uses serially connected´ legs or any symmetrical legs.

The present invention is based on two parallel multipliers, one using larger capacitors charged in parallel and discharged in series and utilizing MEMS switches and the other multiplier using continuously clocked diode switched smaller capacitors to keep the output voltage constant when the output signal is active.

We have shown that the present invention is not obvious regardless of any combination of prior art the Examiner is referring to when rejecting the innovativeness of the present invention.

Note especially that the Kowshik specification just like the Soneda specification never mentions MEMS switches nor charge conservation. Both specifications separately differ significantly from the present invention and no combination of their features will lead anybody to the present invention.

The present inventive voltage multiplier will work with any kind of switches, but one inventive feature is that the invented circuit allows the use of MEMS switches, and this use of MEMS elements is of great economic advantage when producing miniature handheld terminals.

Neither Kowshik nor Soneda discloses use of micromechanical (MEMS) switches. Applicant states the following at page 1, line 32 to page 2, line 2 of Applicant's specification:

> An example of an improved variant of the Marx multiplier called the Mosmarx multiplier was given by P.E.K.Donaldsen: "The Mosmarx voltage multiplier", Electronics & Wireless World, August 1988, pages 748-750. Here metal oxide semiconductors (MOS) switches were used instead of spark gaps. When continuous output is needed high voltage charge is stored in a separate reservoir capacitor, isolated by a serial diode from the output stage, and the switches are operated continuously. The continuous operation prevents the use of micromechanical (MEMS) switches which have a limited lifetime and/or operating frequency.
>
> Applicant further states the following:
>
> Further, the first voltage multiplier 21 may be of any switching capacitor circuit type suitable for use in voltage multipliers, and the second multiplier 22 can for example be of Crockton-Walton type, but also be of any other type of diode-chain multiplier circuit. Further, instead of semiconductor switches also relays or MEMS (micro electro-mechanical system) switches may be advantageously be used to operate at least the multiplier 21.
>
> In the foregoing a novel method of interconnecting only slightly modified standard voltage multipliers has been presented giving numerous advantages, like decreasing the size of the needed capacitors, and enabling cost effective solutions like the use of MEMS switches, ***hitherto not used in voltage multipliers***, to be employed in future handheld terminals.

Page 7, line 30 to page 8, line 3 (emphasis added) of Applicant's specification. Thus, an exemplary advantage of the disclosed invention is that an embodiment allows the use of MEMS switches.

Because neither Kowshik nor Soneda (nor their combination) discloses that MEMS switches may be used for switches in a switching capacitor circuit and because the Applicant has shown an embodiment able to use MEMS switches when such switches were not used before in such a configuration, Applicant respectfully submits that dependent claim 3 is patentable over Kowshik in view of Soneda.

CLAIM 4

The Patent Office has not addressed the merits of claim 4. Claim 4 recites "Capacitive voltage multiplier according to claim 1, characterised in that the output of the switching capacitor circuit (21) is activated at the start of a control pulse." Kowshik does not disclose a switching capacitor circuit. With regard to the combination of Kowshik and Soneda, it is unclear as to how Soneda would operate in conjunction with Kowshik.

The operation of a combination of Kowshik and Soneda is unclear and basically undefined. Furthermore, the Examiner has made no rejections or comments as to how a combination of Kowshik and Soneda would operate. As there is no disclosure or implication in either Kowshik or Soneda (or their combination) of "the output of the switching capacitor circuit (21) is activated at the start of a control pulse", this claim is patentable over the combination of Kowshik and Soneda.

CLAIM 5

The Patent Office has not addressed the merits of claim 5. Claim 5 recites "Capacitive voltage multiplier according to claim 4, characterised in that an output of the switching capacitor circuit (21) is not coupled via a diode to the output terminal (32) of the multiplier so that current at the end of the control pulse can flow back into the pump capacitors, whereby the charge in the load capacitor is partly restored in the pumping capacitors."

Dependent claim 5 recites that the "output of the switching capacitor circuit (21) is not coupled via a diode to the output terminal (32) of the multiplier" (emphasis added). As seen in Figs. 1 and 11 of Applicant's specification, the output of the switching capacitor circuit (21) is not coupled to the output terminal (32) of the multiplier through a diode. As disclosed by Applicant, an intended use of an exemplary embodiment is for displays, where

the not insignificant parasitic capacitance 103 of the display itself contains a charge too, which will also be recovered when using an exemplary embodiment of the present disclosure, page 5, lines 6-14.

In contrast, Kowshik discloses that diodes are connected, as part of the output stage 204, between the output V_{pp} and capacitors (e.g., C_A-C_C and/or C_1-C_N) of the charge pump circuit.

Further, Soneda discloses the output of the internal power supply is provided through a transistor configured as a diode, PTL.

Consequently, dependent claim 5 in combination with the features of independent claim 1 is further patentable over Kowshik and Soneda.

CLAIM 6

The Patent Office has not addressed the merits of claim 6. Claim 6 recites "Capacitive voltage multiplier according to claim 4, characterised in that the diode chain circuit (22) is continuously operated during the control pulse duration and holds the output voltage at a fixed level." It is noted that a control pulse is used to enable the switching capacitor circuit (21) and high voltage should be produced during the control pulse duration. See Applicant's specification at pate 7, lines 4-12.

The Patent Office has given no indication of how a combination of Kowshik and Soneda would operate.

As neither Kowshik or Soneda alone discloses or implies the subject matter of claim 6, the combination of Kowshik and Soneda does not disclose or imply this subject matter. For at least these reasons, claim 6 is patentable over the combination of Kowshik and Soneda.

CLAIM 7

The Patent Office has not addressed the merits of claim 7. Claim 7 recites "Capacitive voltage multiplier according to claim 1, characterised in that the diode chain circuit (22) output is through a diode (102) and that no reservoir capacitor is used."

Claim 7 is allowable at least for the reasons base claim 1 is allowable.

CLAIM 8

The Patent Office has not addressed the merits of claim 8. Dependent claim 8 recites "Capacitive voltage multiplier according to claim 1, characterised in that a supply voltage input diode (101) is used for the switching capacitor circuit (21) allowing the initial voltage of the pump capacitors to be higher than the incoming supply voltage."

Claim 8 is allowable at least for the reasons base claim 1 is allowable.

CONCLUSION

For at least the above reasons, the Applicant/Appellant contends that claims 1-8 are patentable over the combination of Kowshik and Soneda. The Applicant/Appellant respectfully requests the Board reverse the final rejections, and further that the Board rule that the pending claims are patentable over the cited art.

Respectfully submitted:

HARRINGTON & SMITH, PC

Walter Malinowski — October 15, 2007
Walter Malinowski — Date
Reg. No.: 43,423

CERTIFICATE OF MAILING

I hereby certify that this correspondence is being deposited with the United States Postal Service as first class mail in an envelope addressed to: Commissioner for Patents, P.O. Box 1450, Alexandria, VA 22313-1450.

Ann Okrentowicz — 10-15-07
Name of Person Making Deposit — Date

(8) CLAIMS APPENDIX

1. Capacitive voltage multiplier for generating voltage pulses, preferably up to 100 V, that are higher than the supply voltage for displays, non-volatile memories and corresponding units especially in small electronic devices, such as handheld telecommunication terminals or corresponding devices,

wherein the multiplier comprises a switching capacitor circuit (21) coupled between input (31) and output (32) terminals of the multiplier, said switching capacitor circuit (21) provided with capacitors and switches for charging the capacitors in parallel and discharging them in series in order to deliver a high voltage pulse,

characterised in that the multiplier further comprises a diode chain circuit (22) coupled between said input (31) and output (32) terminals of the multiplier, said diode chain circuit (22) comprising a diode-chain and pumping capacitors for delivering high voltage current.

2. Capacitive voltage multiplier according to claim 1, characterised in that when high voltage pulse is desired in the switching capacitor circuit (21) the series coupling switches (odd) are activated by a control pulse and all other switches (even) are opened and that in stand-by mode (no pulse) the series coupling switches (odd) are open and all other switches (even) are closed in order to charge the pump capacitors from the supply voltage, and that charge sharing will occur with the charge including the load capacitance (103).

3. Capacitive voltage multiplier according to claim 1, characterised in that the switches of the switching capacitor circuit (21) are MEMS switches.

4. Capacitive voltage multiplier according to claim 1, characterised in that the output of the switching capacitor circuit (21) is activated at the start of a control pulse.

5. Capacitive voltage multiplier according to claim 4, characterised in that an output of the switching capacitor circuit (21) is not coupled via a diode to the output terminal (32) of the multiplier so that current at the end of the control pulse can flow back into the pump capacitors, whereby the charge in the load capacitor is partly restored in the pumping capacitors.

6. Capacitive voltage multiplier according to claim 4, characterised in that the diode chain circuit (22) is continuously operated during the control pulse duration and holds the output voltage at a fixed level.

7. Capacitive voltage multiplier according to claim 1, characterised in that the diode chain circuit (22) output is through a diode (102) and that no reservoir capacitor is used.

8. Capacitive voltage multiplier according to claim 1, characterised in that a supply voltage input diode (101) is used for the switching capacitor circuit (21) allowing the initial voltage of the pump capacitors to be higher than the incoming supply voltage.

END OF CLAIMS

(9) EVIDENCE APPENDIX

There is no evidence submitted pursuant to 37 C.F.R. §§1.130, 1.131, or 1.132 or entered by the Examiner and relied upon by Appellant.

(10) RELATED PROCEEDING APPENDIX

There are no known decisions rendered by a court or the Board in any proceeding identified pursuant to paragraph (c)(1)(ii) of 37 C.F.R. §41.37.